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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/725,566	12/03/2003	David Robert Cameron Rolston	16005-3US-1 JA/lm	3996
20988	7590	04/03/2006	EXAMINER	
OGILVY RENAULT LLP 1981 MCGILL COLLEGE AVENUE SUITE 1600 MONTREAL, QC H3A2Y3 CANADA			PHAN, THIEM D	
			ART UNIT	PAPER NUMBER
			3729	
DATE MAILED: 04/03/2006				

Please find below and/or attached an Office communication concerning this application or proceeding.

SR

Office Action Summary	Application No.	Applicant(s)	
	10/725,566	ROLSTON ET AL.	
	Examiner	Art Unit	
	Tim Phan	3729	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 09 September 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) 18 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-17 is/are rejected.
- 7) ☒ Claim(s) 19 and 20 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>11/26/04</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Title

1. The following title is suggested: "Method for Manufacturing an Optoelectronic Package".

Specification

2. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required: In Claim 3, there is a limitation step of polishing the substrate, which is neither described nor referred to in the specification and drawings. Proper correction is required.

Claim Objections

3. Claim 18 is objected to because of the following informalities: a claim cannot depend on itself as it cannot further limit the subject matter of a previous claim. Accordingly, the claim has not been treated on the merits. Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claim 3 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The claimed language "... polishing of said substrate ..." is confusing and unclear. This language is held to be vague and indefinite. This language does not convey to the reader that the invention does comprise a step of polishing the coating substance as disclosed in the specification.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. Claims 1, 2, 6, 7 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nishimori et al (US 5,107,327).

As applied to claim 1, Nishimori et al teach a method of making photosemiconductor device, comprising:

- providing a substrate (Fig. 5, 11);
- securing an optoelectronic chip (Fig. 5, 13) on said substrate;
- providing a translucent coating substance (Fig. 5, 16; Abstract) over the optoelectronic chip; and
- regulating the thickness (Fig. 15, 1; col. 8, lines 66+) of the translucent coating substance to create a planar surface over at least said optoelectronic chip, substantially parallel to said substrate; wherein said planar surface over said optoelectronic chip provides an optical coupling window, except for directly claiming the step of polishing the translucent coating substance.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to consider the step of polishing the translucent coating substance in order to regulate the thickness of the translucent coating substance for optical unevenness control and it is also known in the art that many polishing steps are performed to remove the surface roughness (Col. 3, lines 6-63; col. 8, lines 20-22).

As applied to claim 2, Nishimori et al teach a method of making photosemiconductor device, including the molding of the photosemiconductor chip within a transparent resin (Fig. 5, 16; Abstract), which obviously surrounds the optoelectronic chip and has a lower hardness than the molding frame to be reused.

As applied to claims 6 and 7, Nishimori et al teach the wire bonding (Fig. 5, 18) from the chip to the substrate.

As applied to claim 10, Nishimori et al teach a transparent epoxy (Abstract).

8. Claim 3, as best understood, is rejected under 35 U.S.C. 103(a) as being unpatentable over Nishimori et al in view of Nishio (US 5,791,973).

Nishimori et al teach a method of making photosemiconductor device, including the step of polishing the translucent resin (Col. 3, lines 6-63; col. 8, lines 20-22) for surface roughness removal, which reads on applicants' claimed invention.

Nishio teaches a method for high precision polishing a substrate with a holding apparatus (Fig. 1, 15A) in order to enable equal polishing to all surface of the substrate.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the two teachings by applying the high precision polishing process, as taught by Nishio, to the method of making photosemiconductor device, as taught by Nishimori et al, in order to enable equal polishing to the surface of the coating resin.

9. Claims 4, 5, 8 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nishimori et al in view of Fjelstad (US 6,583,444).

Nishimori et al teach a method of making photosemiconductor device, including a step of securing the optoelectronic chip (Fig. 15, 13) with an adhesive (Fig. 15, 12) to the substrate (Fig.

15, 11), which reads on applicants' claimed invention.

Fjelstad teaches a method of making microelectronic package with an electrically conductive adhesive (Fig. 12E, 742) between the chip (Fig. 12E, 740) and the substrate (Fig. 12A, 720), which can be dielectric (Fig. 12A, 722) or ceramic and with peripheral trace lines (Fig. 12F, 746 & 736) in order to provide a common ground plane to all the chips.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the two teachings by applying the electrically conductive adhesive, as taught by Fjelstad, to the method of making photosemiconductor device, as taught by Nishimori et al, in order to enable a common ground plane to many chips.

10. Claims 11-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nishimori et al in view of Miura et al (US 6,170,996).

As applied to claims 11 and 16, Nishimori et al teach a method of making photosemiconductor device, including a step of applying a liquid form resin over said optoelectronic chip and is allowed to harden or to mold (Fig. 5, 16; Abstract), wherein said polishing is performed varying the resin thickness (Fig. 5, 1; col. 3, lines 6-63; col. 8, lines 20-22), in order to create a planar surface over at least said optoelectronic chip, substantially parallel to said substrate, which reads on applicants' claimed invention.

Miura et al teach a method of making optical module encapsulated with resin with the resin being applied in liquid form as a bead (Fig. 4B, 18) in order to apply gravity for slow resin filling without incurring any air bubble space during the filling.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the two teachings by applying the resin filling, as taught by Miura et al, to the method of making photosemiconductor device, as taught by Nishimori et al, in order to apply gravity for slow resin filling without incurring any air bubble space during the filling.

As applied to claims 12, 14 and 17, Nishimori et al teach the buffing of the coating resin (Col. 3, line 62).

As applied to claim 13, Nishimori et al teach the encapsulated wirebonds (Fig. 5, 18).

As applied to claim 15, Nishimori et al teach the transparent, epoxy resin of bisphenol A (Col. 6, lines 60 & 61), which is moisture resistant.

Allowable Subject Matter

11. Claims 19 and 20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicants' disclosure.


Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tim Phan whose telephone number is 571-272-4568. The examiner can normally be reached on M - F, 9AM - 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Peter Vo can be reached on 571-272-4690. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tim Phan
Examiner
Art Unit 3729

tp
March 30, 2006



**A. DEXTER TUGBANG
PRIMARY EXAMINER**